Fuseless Shunt Y Capacitor Bank Protection & Control
Applying the BCD per the IEEE C37.99

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In today's deregulated market, with an influx of independent power producers adding megawatts to existing lines, utilities are discovering that transmission bottlenecks, rather than a shortage of generation, are limiting their ability to efficiently deliver power. An effective solution to this problem is to add shunt capacitance at strategic locations to increase the power factor, reduce I^2R losses and provide voltage and var support to heavily loaded lines.

Capacitor banks require special protection schemes to detect failures of the individual elements that compose the capacitor unit (can). While bank design is a consideration, the same principles apply to externally fused, internally fused and fuseless capacitor banks, with the latter requiring greater sensitivity. This paper will focus on the protection of fuseless wye shunt capacitor banks and specifically how the ZIV type BCD-G terminal can be applied according to the IEEE C37.99-2000 *Guide for the Protection of Shunt Capacitor Banks.*

Capacitor bank design has evolved over the years to produce smaller and more reliable designs. The latest technology uses fuseless capacitors in series strings to compose modern bank designs. Fuseless capacitors utilize sophisticated, polypropylene film and advanced dielectric fluids making them much less susceptible to case ruptures than their kraft paper and PCB predecessors. The internal design of fuseless capacitors is similar to externally fused capacitors, which are configured with a few elements in parallel and many elements in series in each unit. Fuseless type banks provide the following economical and technical advantages.

- Space requirements are reduced since there is no need for external fuses, fuse rail assemblies, insulators, etc.
- The bank configuration of fuseless banks typically requires a smaller footprint
- Reduced maintenance due to increase reliability of the individual cans
- Fewer spare parts to stock
- Reduced failure damage to adjacent substation devices

The failure mode of an element in a fuseless type unit is to create a physical weld, and thus provide an electrical short on the circuit. The shorted circuit is capable of carrying full capacitor rated current and consequently reduces the capacitance of the parallel elements in the group. This reduction of capacitance translates to an increased voltage level on the remaining healthy elements in the unit. Standards and manufactures' recommendations indicate that the voltage applied on each unit should not exceed 110% of the rated value.

A resulting element failure will also produce a shift at the neutral point of the capacitor bank. The shift in capacitance will create a proportional shift in the neutral to ground voltage. This is referred to as an unbalance voltage and can be calculated from the design parameters of the capacitor bank. An unbalance protection scheme can be utilized to detect this shift of neutral to ground voltage and respond accordingly. The ZIV type BCD-G responds to the unbalance voltage for ungrounded and grounded capacitor banks and can be used in unbalance protection schemes.

As indicated in the C37.99, unbalance protection is used to:

- Trip the bank promptly if an unbalance indicates the possible presence of external arcing or cascading fault within the capacitor bank
- Provide early unbalance alarm signal(s) to indicate the failure of capacitor elements (or operation of fuses for internally or externally fused banks)
- Trip the bank for unbalances large enough to indicate that continuing operation may result in:
  - Damage to remaining good capacitor units or elements from overvoltage
  - Fuse malfunction (for fused banks)
  - Inappropriate filter operation (for filter banks)
  - Other undesirable consequences

Failure to provide adequate unbalance protection may lead to one or more of the following situations:

- Excessive Damage to the capacitor bank
- Adverse system effects
- Spread of damage to adjacent equipment
- Excessive period when the damaged equipment is unavailable
- Possible case rupture and undesirable discharge of dielectric liquid and/or fire

The nominal unbalance voltage at the neutral of an ideal capacitor bank will be zero, indicating a *balanced* system. In reality, manufacturing tolerances of the individual capacitor units as well as native system unbalance will produce a nominal unbalance voltage at the neutral point. To eliminate this nominal *unbalance*, a utility would have the time-consuming task of rebalancing their loads and/or redistributing the capacitor units to achieve a nominal zero unbalance voltage. Failing to do this would mean that the utility would have to account for the nominal voltage unbalance at the neutral point and increase their settings accordingly. This adjustment of settings would reduce the sensitivity of the unbalance protection scheme.

However, the BCD-G model incorporates an unbalance compensation function that eliminates the need to reconfigure the system or the bank to achieve ideal sensitivity. The relay internally sums the three phase potentials to achieve a $3V_0$ quantity. This quantity is then compared to the zero sequence voltage at the capacitor bank neutral. Any shift in the bus potentials will be reflected in the neutral and will be self-canceling in the algorithm.

Additionally, by initiating the password protected calibration function, the relay will automatically detect the inherent unbalance voltage applied to the neutral point due to manufacturing tolerances of the individual units that compose the capacitor bank. This value is then nulled out during commissioning, and from this point forward, any unbalance at the neutral point can be attributed entirely to capacitor element failures.

Another consideration concerning unbalance conditions is harmonics, especially in areas that are susceptible to geomagnetic induced currents (GIC). The BCD applies a digital filter to remove the harmonic content of the unbalance signal for protection functions. However, this filter is applied only to the protection elements, allowing the user to examine the harmonic content in the oscillographic wave capture functions included in terminal.

The fuseless capacitor design inherently requires sensitive protection since the goal is to detect individual failures of capacitive elements *within* each can. As fuseless banks are sized for larger voltages, the number of capacitor elements in series increases and, consequentially, the shift in voltage unbalance for each element failure decreases. According to the equation $V_{unb} = E/(E-1)$, a bank with 40 elements in series (for example 8 cans consisting of 5 series elements each) only experiences 2.6% overvoltage (40/39) for a single element failure, while a bank with 20 elements in series experiences 5.3% overvoltage (20/19) for a single element failure. In both cases, a single element failure does not produce a 10% overvoltage so the bank can safely remain in service, but the loss of an element should be detectable and a corresponding alarm should be generated.

The following guidelines, as per the IEEE C37.99, should be considered when calculating unbalance settings:

- The unbalance trip time delay should be minimized to reduce damage from arcing faults within the bank structure and reduce damage to CTs, VTs and relay systems for single phase or open phase conditions.
- The unbalance trip time delay should be long enough to avoid false operations due to:
    - Inrush
    - System ground faults
    - Switching of nearby equipment
    - Non-simultaneous pole operation of the energizing switch

  0.1 seconds is adequate for most applications.
- For grounded banks, coordination with system ground relays should be considered in the event of an open pole or single phasing.
- A delay may need to accommodate protection system settling time upon initialization.
- A lockout feature should be provided to prevent inadvertent closing of the capacitor bank after an unbalance trip.
- To allow for the effects of inherent unbalance, the trip setting should be halfway between the critical step (element failure) and the next lower step.
- The lockout relay should de-energize the voltage relay for switch failure or single phasing conditions.
- The maximum system operating voltage, with the capacitor bank energized, should be used for setting unbalance relays.

Using a ZIV provided spreadsheet based on the C37.99, a user can determine the overvoltage on the healthy elements in the unit and the voltage unbalance developed on the capacitor bank neutral from each element failure. The BCD-G is equipped with three set points to respond to different conditions. For a single element failure (Level 1), the relay will send a latched alarm to alert operations personnel of a problem in the bank so appropriate maintenance to examine the bank can be scheduled. For a 10% overvoltage (Level 2), the relay will trip the bank with a time delay to ensure a valid unbalance condition and avoid nuisance tripping. For a larger overvoltage (Level 3), indicating a possible cascading or catastrophic failure, the relay should be set to trip the bank with minimal time delay.

The table in Figure 1 below is a model of a capacitor bank and is designed to demonstrate how the bank will respond for each subsequent element failure. In the example shown in Figure 1, the bank design (size, voltage, etc.) is displayed in the top left portion of the spreadsheet. The capacitor bank per-unit values are displayed in the middle portion of the spreadsheet, with the legend for the columns located in the top right portion. The per-unit values are calculated into system values in the lower portion of the spreadsheet.

Fuseless Capacitor Banks, Wye Connected

Cap Bank Design	
Rated Cap Bank Voltage V L-L in kV	69
System Voltage V L-L in kV	69
Bank Size (MVAR)	11.0
VT Ratio XX / 1	350
VT Neutral Ratio XX / 1	166
K (VT Scale Factor)	0.47
CT Ratio XX / 1	N/A
CT Neutral Ratio XX / 1	N/A
Neutral to GND Resistor	N/A
Xc per string	432.8
Total Bank Phase Current	92.15
Voltage (line to neutral)	39.84

Legend	
e	Shorted elements
Cst	String per unit capacitance
Cy	Affected wye capacitance
Cp	Affected phase capacitance
Vng	Neutral to ground voltage (pu of Vlg)
Vln	Voltage on affected phase
Ve	Voltage on affected elements
Vunb	Unbalance voltage
Vunb-sec	Secondary unbalance voltage
Ig-pri	Zero sequence current
Ig-sec	Secondary zero sequence current
BCD-G Vin	Voltage input to protective relay

Series elements, phase to neutral	24	E
Parallel Strings per phase	2	Sp
Parallel Strings per phase, left wye	2	Sl
0 = grounded, 1 = ungrounded	1	G

Per Unit Values

e	Cst	Cy	Cp	Vng	Vln	Ve
0	1.000	1.000	1.000	0.000	1.000	1.000
1	1.043	1.022	1.022	0.007	0.993	1.036
2	1.091	1.045	1.045	0.015	0.985	1.075
3	1.143	1.071	1.071	0.023	0.977	1.116
4	1.200	1.100	1.100	0.032	0.968	1.161
5	1.263	1.132	1.132	0.042	0.958	1.210
6	1.333	1.167	1.167	0.053	0.947	1.263
7	1.412	1.206	1.206	0.064	0.936	1.321
8	1.500	1.250	1.250	0.077	0.923	1.385
9	1.600	1.300	1.300	0.091	0.909	1.455
10	1.714	1.357	1.357	0.106	0.894	1.532

System Values

e	Ve	Vunb	Vunv-sec	Ig - pri	Ig-sec	BCD-G Vin
0	1.000	0.0	0.00	#REF!	#REF!	0.00
1	1.036	286.6	1.73	#REF!	#REF!	0.82
2	1.075	594.6	3.58	#REF!	#REF!	1.70
3	1.116	926.5	5.58	#REF!	#REF!	2.65
4	1.161	1285.1	7.74	#REF!	#REF!	3.67
5	1.210	1673.9	10.08	#REF!	#REF!	4.78
6	1.263	2096.8	12.63	#REF!	#REF!	5.99
7	1.321	2558.4	15.41	#REF!	#REF!	7.31
8	1.385	3064.5	18.46	#REF!	#REF!	8.76
9	1.455	3621.7	21.82	#REF!	#REF!	10.35
10	1.532	4238.1	25.53	#REF!	#REF!	12.11

Example
TS091602

The System Values portion of the table is used to make settings calculations. The column labeled “e” represents the number of failed capacitor elements. The column labeled “Ve” represents the percentage of overvoltage on the remaining healthy elements in the unit. The column labeled “Vunb” represents the primary voltage unbalance value. The column labeled “Vunb-sec” represents the secondary voltage unbalance value. The last column, “BCD-G Vin,” represents the voltage unbalance seen at the relay after PT compensation is applied. The remaining two columns are utilized for grounded capacitor bank applications and consequently display a reference error in this example.

Figure 1

From this example, a single element failure (e=1) creates a 3.6% overvoltage on the healthy elements in the unit. Consequently, 286.6 volts primary will be developed at the neutral point, which is detected as 0.82 volts secondary at the relay. As such, the Level 1 Voltage Unbalance setting should be somewhat less than 0.82 V to detect a single element failure and trigger an alarm. In accordance with the C37.99, it is recommended that the time delay for the alarm should be long enough to avoid operation during system faults or temporary overvoltage, yet short enough to minimize the probability of compensating failures yielding an ambiguous indication. Ten seconds is usually an appropriate delay for the alarm.

Likewise, the loss of three elements (e=3) represents the critical step and creates an overvoltage of 11.6% on the healthy elements in the unit, developing 2.65 volts secondary at the relay. The relay should be set about half way between 2.65 and 1.70 volts secondary as these voltages represent the critical step and preceding step respectively, per the C37.99 recommendations.

For voltage unbalance magnitudes larger than an entire can failure, the relay should be tripped with minimal time delay to reduce the possible rapid escalation of damage. The C37.99 recommends a time delay of 0.01 – 0.05 seconds. This delay, coupled with the times associated with the lockout relay and breaker operation may result in a total clearing time on the order of 0.1 second.

Bank design and configuration will directly impact the unbalance voltage created from an element failure. In any installation, the protection should trip the bank when all of the elements in a unit have failed, regardless of the voltage unbalance magnitude. In banks that have eleven or more units in series, the failure of a unit would not create a 10% overvoltage on the remaining units, but the relay should be set to trip for this condition, as per the C37.99.

Another protection factor to consider is the physical location of the capacitor bank in the substation. Voltage from adjacent lines can stray inductively into the bank or into an unshielded cable connecting the secondary of the voltage-sensing device to the input of the relay when an ungrounded capacitor bank is switched open. The magnitude can be large enough to create a Level 3 Voltage Unbalance. The natural response of the BCD-G is to issue a minimal time delayed trip command for this level of unbalance.

To accommodate for this situation, the BCD-G has been designed with a blocking logic that monitors the breaker status by measuring the current and the "b" contact of the switching device. If the current level on all phases is below a set threshold, or if an open breaker status is detected the voltage unbalance tripping is blocked until the current level is exceeded and the breaker status changes, indicating a closed breaker.

However, at many voltages, circuit switchers rather than circuit breakers are responsible for capacitor bank switching. Monitoring the breaker status by contacts is not sufficient for circuit switchers, as the contacts may not indicate the actual status with adequate time resolution due to the time associated with the blade travel.

In substations where circuit switchers are used and stand-alone CTs are not available for the voltage unbalance trip blocking function, another solution is available. Voltage unbalance trip blocking for these cases can be performed by logic developed utilizing programmed inputs and outputs in the ZIVercom® communications software. ZIVercom® is a Windows™ based, intuitive settings, programming and communications software. Through this tool, the user can monitor the contacts of the circuit switcher and add appropriate time delays ensure the appropriate blocking of the voltage unbalance trip signal.

Aside from protecting the capacitor bank from overvoltage due to element failures, the C37.99 also recommends providing primary system protection to reduce stresses and minimize damage to capacitors for the following events:

- External arcing
- Overvoltages, including harmonic distortion
- Bank overcurrent
- Loss of bus voltage
- System overvoltage
- Other considerations (PT fuse failure, breaker failure protection, surge arrestor protection)

Voltage units in the BCD-G provide system protection for overvoltage, undervoltage and loss of bus potential protection. Additionally, current units provide bank overcurrent protection. The BCD is also equipped with PT fuse failure detection and breaker failure protection. The voltage unbalance input is designed to withstand surges for grounded applications that utilize a burden resistor in series with the secondary circuit of the neutral to ground CT.

External arcing may cause case ruptures or other damage to capacitor units if not tripped promptly. While unbalance protection is considered the primary protection for this condition, the C37.99 recommends redundant protection for extremely large banks in the form of current unbalance or negative sequence current protection.

Another consideration, unique to capacitor banks, is the frequent switching duties. Many utilities control capacitor banks via switching commands from their SCADA system. However, the BCD is also equipped with a built-in automatic control function for installations not connected to SCADA systems or for utilities that implement a PLC for control. The automatic control function performs switching operations based on either time-biased voltage settings or by monitoring reactive power on an adjacent transformer or bus.

Using the time-biased voltage control option, the user can select the voltages to switch the capacitor bank in (V_{add}) or out (V_{remove}) based on time settings. A dead-band setting also accounts for the voltage step change associated with switching the bank in or out to avoid a toggling condition. If a significant voltage drop occurs, the bank will be switched open and locked out to prevent energizing a transformer with a bank in service (V_{off}).

The capacitor bank can also be controlled by monitoring the reactive power on an adjacent transformer or bus. The user selects the connection and disconnection Var settings. The control is supervised by the V_{off} setting.

There are other shunt capacitor bank protection schemes indicated in the C37.99. The alternative most used is the voltage differential scheme. Besides the inherent sensitivity of a differential scheme, another perceived advantage to this scheme is faulted phase indication. However, the recommended maintenance practice is to measure the capacitance of each series string (all units in externally and internally fused designs), as distributed failures and ambiguous conditions may not be accurately detected or indicated by either method. Additionally, the actual time required

to detect which phase(s) and unit(s) the failure(s) is located is typically small in comparison to the time required for a crew to travel to the substation.

Utilizing the unbalance protection scheme incorporated in the BCD-G provides economic benefits over other schemes. The unbalance scheme utilizes the existing bus PTs and requires only one additional voltage-sensing device in the capacitor bank neutral. The sensitivity provided by the voltage unbalance compensation, the reduced cost of fewer required instrument transformers combined with the system protection and automatic control functions makes the BCD-G a complete, reliable, and economic solution for most capacitor bank protection and control applications.

By strategically implementing properly protected shunt capacitor banks, utilities can increase their capacity and voltage support in heavy loading conditions. The flexibility of the BCD-G maximizes the availability of capacitor banks because the protection is sensitive enough to allow scheduled maintenance for minor problems while keeping the bank in service, with the piece of mind that the relay will trip the bank if additional problems occur. When tripping does occur, the BCD-G equipped with a host of software and analysis tools to assist in determining the cause.

It should be noted that ***this relay was designed and has been successfully applied to a variety of capacitor bank designs, connections and voltage levels***. The fuseless design was chosen for this application guide since it typically requires the most stringent and sensitive protection. If you have a new or existing bank that you would like to protect with a BCD, please consult one of our application engineers with the specifics of your bank and the corresponding PT and CT ratios and switching device information.

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Tyson J. Salewske received his BSEE from Iowa State University in 1998 and has been employed as an application engineer with ZIV USA, Inc. since graduation. Tyson has been involved with the various protection and integrated protection and control projects throughout his tenure at ZIV. However, his greatest interest has been in the area of capacitor bank protection and control. He has presented information on this topic to over 30 of the largest utilities in the US as well as at the 2001 IEEE PES in Atlanta. As an IEEE member, Tyson attends a variety of IEEE and PSRC conferences each year.